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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,530	03/31/2004	Russell Rapport	254-094-CIP4-C1	6898

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EXAMINER	
TRAN, THANH Y	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 12/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/814,530	RAPPORT ET AL.	
	Examiner	Art Unit	
	Thanh Y. Tran	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) *13--31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/26/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because there is no figure showing the relations between upper flex contact 42 and lower flex contact 44 (first and second flex contacts) as recited in claims 2, 3, 4, 7, 9, 10, 11 and 12. There is no figure showing both elements 42 and 44 as described in the specification of the invention and as recited in the claims. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 9, 11 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 9, it is also unclear to the Examiner if the functional language "express an n-bit datapath" and "express a 2n-bit module datapath" are functions inherent to the structure already recited (for example, what kind of CSP contact is used to express an n- bit datapath) or does this functional language imply additional structural limitation not explicitly stated in the claim. Applicant is required to clarify. For applying art the Examiner assumes that the functions of "express an n-bit datapath" and "express a 2n-bit module datapath" are inherent to the already cited structure.

Claim 11 is unclear as to what Applicant means by "on-pad vias"?

Claim 12 is unclear as to what Applicant means by "off-pad vias"?

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1 and 3-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Mukerji et al (U.S. 6,300,679).

As to claim 1, Mukerji discloses in figure 5 a high-density circuit module comprising: a first CSP (chip 501) having upper and lower major surfaces and a first and a second edge, the edges delineating a lateral extent for the upper major surface; a second CSP (chip 502); a form standard (mask 512) disposed between the first and second CSPs (501, 502), the form standard (mask 512) having a lateral extent greater than the lateral extent of the upper major surface of the first CSP (501), the form standard (mask 512) presenting at least one surface for contact with flex circuitry (comprising elements 510 and 511), the flex circuitry connecting the first and second CSPs (501, 502) and disposed to place a first portion of the flex circuitry beneath the lower major surface of the first CSP (501) and a second portion of the flex circuitry above the form standard (mask 512) disposed between the first and second CSPs (501, 502).

As to claim 3, Mukerji discloses in figure 5 a high-density circuit module in which the flex circuitry (comprising elements 510 and 511) comprises a conductive layer (trace 511) that expresses first and second flex contacts (first and second flex contacts are flex contacts 511 bonded to corresponding balls 530) for connection of the first and second CSPs (501, 502).

As to claim 4, Mukerji discloses in figure 5 a high-density circuit module comprising: flex circuitry (comprising elements 510 and 511) having at least one conductive layer (511), an outer layer (510), and first and second flex contacts (first and second flex contacts are flex contacts 511 bonded to corresponding balls 530); a first CSP (chip 501) having CSP contacts (530), the CSP contacts (530) of the first CSP (501) contacting the flex circuitry; a form standard (mask 512) presenting at least one surface for contact with the flex circuitry; a second CSP (502) having CSP contacts (chip 520), the first CSP (chip 501) being disposed above the form standard

(mask 512) and the second CSP (chip 502), and the CSP contacts of the second CSP (chip 520) contacting the flex circuitry.

As to claim 5, Mukerji discloses in figure 5 a high-density circuit module in which the form standard (mask 512) presents at least one curved surface for contact with flex circuitry (510, 511).

As to claim 6, Mukerji discloses in figure 5 a high-density circuit module comprising: a first CSP (chip 501) having an upper and a lower major surface and a set of CSP contacts (530) along the lower major surface; a second CSP (chip 502) having first and second lateral edges and upper and lower major surfaces and a set of CSP contacts (520) along the lower major surface, the first and second lateral edges delineating an extent of the upper major surface of the second CSP (502) and the first CSP (501) being disposed above the second CSP (502); flex circuitry (comprising elements 510, 511) connecting the first and second CSPs (501, 502); and a form standard (mask 512) having an extent greater than the extent of the upper major surface of the second CSP (502) and disposed so as to extend between the first and second CSPs (501, 502) and beyond the extent of the upper major surface of the second CSP (502).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2, and 7-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mukerji et al (U.S. 6,300,679) in view of Nicewarner, Jr. et al (U.S. 5,776,797).

As to claim 2, Mukerji does not disclose a high-density circuit module in which the flex circuitry comprises at least one flex circuit having first and second conductive layers, between which there is an intermediate layer, the first and second conductive layers having demarked first and second flex contacts, the first flex contacts in electrical connection with the first CSP and the second flex contacts in electrical connection with the second CSP. Nicewarner discloses in figure 3 a high-density circuit module in which the flex circuitry (as indicated at 40, 42 and 12) comprises at least one flex circuit having first and second conductive layers (40, 42), between which there is an intermediate layer (as indicated at 12), the second conductive layer (42) having demarked first and second flex contacts (22, 28), the first flex contacts (22) in electrical connection with the first CSP (chip 18) and the second flex contacts (28) in electrical connection with the second CSP (chip 24). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the module of Mukerji by having a flex circuit which includes first and second conductive layers and an intermediate layer as taught by Nicewarner for allowing mechanical and electrically attachment between the integrated circuit assemblies (see col. 1, lines 55-65 in Nicewarner).

As to claim 7, Mukerji discloses in figure 5 a high-density circuit module comprising: a first CSP (chip 501) having first and second major surfaces with a plurality of CSP contacts (530) along the first major surface, a second CSP (chip 502) having first and second major surfaces with a plurality of CSP contacts (520) along the first major surface, a form standard (mask 512), the first CSP (501) being disposed above the form standard (mask 512) and the second CSP (502), the form standard (512) presenting an at least one curved surface for contact a pair of flex circuits (a pair of flex circuits are the flex circuits which are from left side and right

side (not shown) of chips 501 and 502, and each comprising elements 510, 511), a conductive layer (trace 511) having demarked a plurality of upper and lower flex contacts (upper flex contacts are upper contacts 511 bonded to corresponding balls 530 of chip 501; lower flex contacts are lower contacts 511 bonded to corresponding balls 530 underneath chip 502), a second set of the plurality of upper and lower flex contacts being comprised of selected ones of upper flex contacts that are connected to corresponding selected ones of lower flex contacts, the plurality of CSP contacts (530) of the first CSP (chip 501) being in contact with the upper flex contacts (upper flex contacts are upper contacts 511 bonded to corresponding balls 530 of chip 501) and the plurality of CSP contacts (520) of the second CSP (502) being in contact with the lower flex contacts (lower flex contacts are lower contacts 511 bonded to corresponding balls 530 underneath chip 502).

Mukerji does not disclose the pair of flex circuits of the form standard each having first and second conductive layers between which conductive layers there is an intermediate layer, the second conductive layer having demarked a plurality of upper and lower flex contacts a set of the plurality of upper and lower flex contacts being connected to the first conductive layer. Nicewarner discloses in figure 3 a high-density circuit module in which the flex circuitry (as indicated at 40, 42 and 12) comprises a flex circuit having first and second conductive layers (40, 42), between which conductive layers there is an intermediate layer (as indicated at 12). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the flex circuit of Mukerji by having first and second conductive layers, between which conductive layers there is an intermediate layer as taught by Nicewarner

for allowing mechanical and electrically attachment between the integrated circuit assemblies (see col. 1, lines 55-65 in Nicewarner).

As to claims 8 and 9, as best understood by Examiner, Mukerji discloses in figure 5 a high-density circuit module comprising a pair of flex circuit (a pair of flex circuits are the flex circuits which are from left side and right side (not shown) of chips 501 and 502, and each comprising elements 510, 511) each of the flex circuits of the pair of flex circuits has supplemental lower flex contacts (lower flex contacts are lower contacts 511 bonded to corresponding balls 530 underneath chip 502) which, in combination with the lower flex contacts, provide connection for the set of module contacts (module contacts are contact balls 530 underneath chip 502).

Mukerji does not disclose a module wherein the first and second CSPs are memory circuits; a data set of the plurality of CSP contacts of the first CSP express an n-bit datapath; a data set of the plurality of CSP contacts of the second CSP express an n-bit datapath: a set of supplemental module contacts to express a 2n-bit module datapath that combines the n-bit datapath expressed by the data set of the plurality of CSP contacts of the first CSP and the n-bit datapath expressed by the data set of the plurality of CSP contacts of the second CSP. Nicewarner discloses in figure 3 a module wherein the first and second CSPs (18, 24) are memory circuits (see col. 1, lines 50-54); a data set of the plurality of CSP contacts (22) of the first CSP (18) express an n-bit datapath; a data set of the plurality of CSP contacts (28) of the second CSP (24) express an n-bit datapath: a set of supplemental module contacts to express a 2n-bit module datapath that combines the n-bit datapath expressed by the data set of the plurality of CSP contacts of the first CSP and the n-bit datapath expressed by the data set of the plurality

of CSP contacts of the second CSP. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the module of Mukerji by having a first and second CSPs are memory circuits as taught by Nicewarner for expressing an n-bit datapath and for storing data or information for a communication device.

As to claims 10, 11 and 12, as best understood by Examiner, Mukerji does not disclose a module wherein the second set of the plurality of upper and lower flex contacts is connected to the first conductive layer with vias that pass through the intermediate layer; the second set of the plurality of upper and lower flex contacts is comprised of upper flex contacts connected to the first conductive layer with on-pad vias; the second set of said plurality of upper and lower flex contacts is comprised of lower flex contacts connected to the first conductive layer with off-pad vias. Nicewarner discloses in figure 3 a high-density circuit module wherein the second set of the plurality of upper and lower flex contacts (22, 28) is connected to the first conductive layer (40) with vias (48) that pass through the intermediate layer (as indicated at 12); the second set of the plurality of upper and lower flex contacts (22, 28) is comprised of upper flex contacts (22) connected to the first conductive layer (40) with on-pad vias (48); the second set of the plurality of upper and lower flex contacts is comprised of lower flex contacts (28) connected to the first conductive layer (40) with off-pad vias (50). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the module of Mukerji by having a plurality of upper and lower flex contacts is connect to first conductive layer with vias that pass through the intermediate layer or with on-pad vias or off-pad vias as taught by Nicewarner for electrically interconnecting the CSP/chip with the first and second conductive layers of the flex circuit.

Double Patenting

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1, 2, 3, 6, 7, 8, 9, 10, 11 and 12 provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 9, 10, 11, 14, 22, 23, 24, 25, 26 and 27 of copending Application No. 10/453,398. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1, 2, 3, 6, 7, 8, 9, 10, 11 and 12 in the present invention having the same/similar meaning/functions/purposes as recited in claims 9, 10, 11, 14, 22, 23, 24, 25, 26 and 27 of copending Application No. 10/453,398.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Gonya (U.S. 6,410,857) discloses signal cross-over interconnect for a double-sided circuit card assembly.

Johnson et al (U.S 5,917,709) discloses multiple circuit board assembly having an interconnect mechanism that includes a flex connector.

Difrancesco (U.S. 5,642,055) discloses electrical interconnect using particle enhanced joining of metal surfaces.

Inaba (U.S. 2001/0040793) discloses electronic device and method of producing the same.

Lee (U.S. 6,614,664) discloses memory module having series-connected printed circuit boards.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TYT

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